

REMARKS

These Remarks are submitted under 35 U.S.C. § 132 and 37 C.F.R. § 1.111 in response to the Office Action mailed December 28, 2005.

Summary of the Examiner's Action and Applicant's Response

The Examiner stated that Claims 1-9 have been allowed. The Examiner has rejected Claim 10 under 35 U.S.C. §102(b), as being anticipated by Anderson, U.S. Patent No. 3,202,937. Applicant respectfully traverses the rejection. Claims 1-10 remain pending.

Response to the Rejection of Claim 10 under 35 U.S.C. § 102(b)

The Examiner rejected Claim 10 under 35 U.S.C. 102(b) as being anticipated by Anderson. The Examiner stated that Anderson discloses a reference circuit for providing a reference voltage only during a predetermined time interval comprising a zener diode (40) for providing the reference voltage in response to a predetermined bias current when the zener diode is reverse biased, and a bias control circuit (36, 34, 26, 30, 24 and 22) for generating the predetermined bias current only during the predetermined time interval. (See FIG. 3). The Examiner stated that the predetermined time interval can be any range of time because it is not specified. The Examiner stated that the discharge time of the capacitor in the circuit shown in FIG. 3 in Anderson indicates that there is a predetermined time period in which the capacitor in the circuit is discharging and providing the reference voltage. Applicant respectfully disagrees.

Applicant respectfully submits that, in the circuit shown in FIG. 3 of Anderson, the capacitor 30 charges via resistor 26 until the voltage across it reaches a peak point corresponding to the sum of the breakdown voltage of zener 34 and the emitter voltage needed to create conduction between the bases B1 and B2 of unijunction transistor 36 (Col. 2, lines 23-45, Col. 3, lines 4-14). When the capacitor voltage reaches that peak point, the emitter current of the unijunction transistor rises rapidly, discharging capacitor 30 through the base B1 of the unijunction transistor 36 and resistor 38 to ground. The resultant rapid rise and fall in current through resistor 38 produces a voltage pulse at terminal 44. Since this circuit is operating as a relaxation oscillator, output pulses continue to be generated in this fashion at terminal 44. The

frequency of these output pulses is dependent on the RC time constant defined primarily by resistor 26 and capacitor 30.

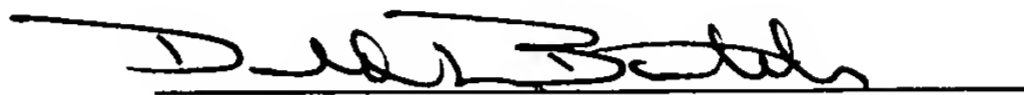
Applicant's understanding of the Examiner's position is that the bias current for zener diode 40 in the circuit in FIG. 3 in Anderson is only provided during the discharge time of capacitor 30 (i.e., when there is conduction between the two bases of unijunction transistor 36), and thus, during a predetermined interval. Applicant respectfully submits, however, that the bias current for zener diode 40 in the circuit in FIG. 3 is not generated only during that discharge interval. That is, the bias current for zener diode 40 is provided in the circuit in FIG. 3 via potential source 22, resistor 24, zener diode 28 and capacitor 42 in order to regulate the voltage at E_1' and the voltage at E_2 **at all times**, i.e., even during the time when there is no conduction between the bases of unijunction transistor 36 (Col. 3, lines 15-20). In contrast to Anderson's circuit, the reference circuit according to the present invention, as claimed in Claim 10, is designed to suppress bias current for the zener diode except during the predetermined time interval when it is needed (Paragraphs 10, 11, and 25). Applicant respectfully submits, therefore, that for the above reasons Anderson does not disclose a bias control circuit for generating a predetermined bias current for a zener diode only during a predetermined time interval, as claimed in Claim 10. Therefore, Applicant respectfully submits that Claim 10 is not anticipated by Anderson.

Conclusion

For the above reasons, Applicant respectfully submits that all pending claims, Claims 1-10, in the present application are allowable. Such allowance is respectfully solicited.

If a telephone conference would expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (415) 984-8200.

Respectfully submitted,



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